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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,164	12/01/2003	Rex M. Teggatz	TI-36323	2069

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EXAMINER	
PATEL, DHARTI HARIDAS	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 01/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/725,164	TEGGATZ ET AL.	
	Examiner	Art Unit	
	Dharti H. Patel	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-13* is/are allowed.

6)☒ Claim(s) *1-7,14,15,27,28 and 30-33* is/are rejected.

7)☒ Claim(s) *16-26,29 and 34-36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 4-5 and 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sander et al., Patent No. 6,853,232. With respect to claim 1, Sander teaches a method [Col. 2, lines 23-26] for controlling a clamping voltage across a terminal of a transistor [Fig. 1, T1] comprising: providing a first clamping voltage in a conductive loop that includes the terminal of the transistor for a first specified period of time [Col. 2, lines 27-32]; reducing the first clamping voltage to an intermediate clamping voltage; holding the intermediate clamping voltage for a specified period of time [Col. 2, lines 32-35]; repeating the reducing and the holding until the intermediate clamping voltage is essentially equal to a final clamping voltage [Fig. 3, UL1].

With respect to claim 4, Sander teaches that the intervals [Fig. 3, Tk, Tab] between clamping voltage levels are different.

With respect to claim 5, Sander teaches that the terminal is a gate of the transistor [Fig. 1, a gate of transistor T1].

With respect to claim 6, Sander teaches that the terminal is a drain of the transistor [Fig. 1, a drain of transistor T1].

With respect to claim 7, Sander teaches that the transistor is a field effect transistor [Fig. 1, T1, Col. 3, lines 44-45].

2. Claims 14-15, 30 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaessler et al., Patent No. 6,772,737. With respect to claim 14, Gaessler teaches a method and circuit system for operating a solenoid valve, the circuit comprises a drive circuit [Fig. 1, 24, 25] coupled to an inductive load [Fig. 1, MV], the driver circuit containing circuitry to control a current built up across the inductive load; and a voltage varying circuit coupled to the driver circuit, the voltage varying circuit containing circuitry to produce a sequence of voltages [Col. 9, lines 11-28].

With respect to claim 15, Gaessler teaches that the sequence of voltages is a decreasing sequence of voltage levels [varying voltages for energizing, holding and de-energizing].

With respect to claim 30, Gaessler teaches that the driver circuit [Fig. 1, 24] is a low-side driver circuit [Driver circuit 24 is coupled to a low side voltage source or ground through switch S2].

With respect to claim 33, Gaessler teaches that a driver circuit coupled to an inductive load is a solenoid mechanism for a vehicle. The solenoid mechanism would be provided in an automotive brake.

3. Claims 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gaessler et al., Patent No. 6,772,737, in view of Mangtani, Patent No. 5,969,964, and further in view of Menegoli, Patent No. 5,834,826. With respect

to claim 27, Gaessler teaches a drive circuit but does not disclose a first high side drive circuit, a second high side drive circuit and a low side drive circuit. Mangtani teaches a high voltage gate driver for a transistor bridge circuit, the bridge power circuit comprises a first high side drive [Fig. 1, IGBT Q1] coupled to a supply voltage source [Fig. 1, +Hv], the first high side drive circuit to permit current from the inductive load [Fig. 1, Ls] to dissipate into the supply voltage source [Col. 1, lines 26-34, lines 40-42]; and a low side drive circuit [Fig. 1, IGBT Q2] coupled to the inductive load [Fig. 1, Ls], the low side drive circuit to regulate the current build up across the inductive load.

However, Mangtani does not disclose a second high side drive circuit coupled to the first high side drive circuit and the current varying circuit, the second high side circuit to allow a voltage drop generated by the current varying circuit to appear in the driver circuit.

Menegoli teaches an integrated circuit that includes elements for driving an inductive load. Menegoli teaches a second high side drive circuit [Fig. 1, 18B] coupled to the first high side drive circuit [Fig. 1, 18A].

All three teachings are related by being drive circuits for driving an inductive load. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Menegoli, which teaches a second high side drive circuit, with the drive circuit of Mangtani in order to form a bridge circuit across high and low power terminals of a power source.

With respect to claim 28, Mangtani teaches that each drive circuit [Fig. 1, Q1 and Q2] comprises a metal oxide semiconductor field effect transistor coupled in parallel with a body diode [Fig. 1, D1 and D2].

4. Claim 31 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gaessler et al., Patent No. 6,772,737, in view of Swize, Publication No. US 2004/0095183A1. Gaessler teaches a driver circuit but does not disclose that the driver circuit is a full H-bridge circuit. With respect to claim 31, Swize teaches an H-bridge driver circuit [Fig. 1, 12] for driving an inductive load [Page 1, paragraph 3].

Both teachings are related by being driver circuits for driving an inductive load. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Swize, which teaches an H-bridge driver circuit, with the driver circuit of Gaessler for the benefit of diverting a current from the high side driver to the low side driver if the voltage exceeds a predetermined level.

5. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gaessler et al., Patent No. 6,772,737, in view of Ribarich et al., Patent No. 5,973,943. Gaessler teaches a driver circuit but does not disclose that the driver circuit is a half bridge circuit. With respect to claim 32, Ribarich teaches a half bridge [Fig. 3, 102, 104] for driving an inductive load [Fig. 3, L1, Col. 2, lines 5-12].

Both teachings are related by being driver circuits for driving an inductive load. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Ribarich, which teaches a half bridge driver circuit, with the driver circuit of Gaessler for the benefit of diverting a current from the high side driver to the low side driver if the voltage exceeds a predetermined level.

Allowable Subject Matter

6. Claims 2-3 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening.

The following is an examiner's statement of reasons for indicating allowance of claim 2: Sander teaches a method for controlling a clamping voltage across a terminal of a transistor but does not disclose that the intervals between clamping voltage levels are equal. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art record.

The following is an examiner's statement of reasons for indicating allowance of claim 2: Sander teaches a method for controlling a clamping voltage across a terminal of a transistor but does not disclose that the first specified period of time and the specified period of time are equal. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art record.

7. Claims 8-13 are allowed. The following is an examiner's statement of reasons for indicating allowance of claim 8. The prior art does not disclose a method for rapidly removing a current from an inductive load without current undershoot comprising: setting a variable current source to produce a first current; holding the variable current source output for a first period of time; checking if a terminating condition is met; setting the variable current source to produce a second current for a second period of time, wherein the second current is smaller than the first current, if the terminating condition is not met; and repeating the checking and the setting. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art record.

8. Claims 16-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for indicating allowance of claim 16: Gaessler et al. teaches a voltage varying circuit but does not disclose that the voltage varying circuit further comprises a variable current source to produce an output current of variable magnitude depending upon an input signal; and a snub resistor coupled in parallel to the variable current source. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

9. Claims 25-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for indicating allowance of claim 25: Gaessler et al. teaches a voltage varying circuit but does not disclose that the voltage varying circuit further comprises a current source; and a serial chain of resistors coupled in parallel to the current source, each resistor is coupled in parallel to a switch, wherein each switch is controlled by a control signal, and wherein an effective resistance of a resistor and switch combination is equal to the resistance of the resistor when the switch is open and is equal to zero when the switch is closed. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

10. Claim 29 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for indicating allowance of claim 29: Mangtani and Menegoli disclose a first high side drive circuit and a second high side drive circuit, but does not disclose that the source terminals of the field effect transistors in the first and second high side drive circuits are coupled together. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

11. Claims 34-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for indicating allowance of claim 34: Gaessler teaches a circuit that comprises a driver circuit and a voltage varying circuit but does not disclose that the circuit further comprises a snub stack coupled in parallel to the driver circuit and the current varying circuit, the snub stack to produce a fixed voltage drop. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through

Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DHP
01/20/2006

PHUONG T. VU
PRIMARY EXAMINER